Homework 4

Due Date: April 14

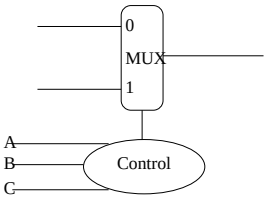
All written homeworks are due at the beginning of class on the due date. There is no provision for homework turned in late. Partial credit will be given for work shown. Points are scaled relative to the "time" value given in the book (the number in square brackets next to the problem). If your homework is longer than one page, please staple or paper-clip the pages together. Be as neat as possible; if I can't read it, it's wrong.

It is not guaranteed that all problems will be graded. We will either cover answers in class and/or a solution sheet will be posted.

At the end of your homework, please write and sign the Honor Code pledge:
I have abided by the Wheaton College Honor Code in this work.

Do text problems (you may want to do the additional problems below **first**):
4.1, 4.5*, 4.7.1*-4.7.3*, 4.7.6*

In addition:



Suppose a three-bit control signal determines the output of a two-input multiplexor, as shown above. If we call the three bits A, B, and C, assume line 1 (true) of the multiplexor is chosen if

`(((A OR B) OR C) OR (A AND C)) OR (A AND B).`

1. [5] Implement the logic for the control signal. Your circuit should directly implement the given expression (do not "optimize" it) using two-input AND and OR gates.
2. [5] Suppose the latency of an AND gate is 28ps (ps = picosecond) and the latency of an OR gate is 35ps. What is the length of the critical path of your circuit?

* Refer to Figure 4.17.